359/Phs.

UG/3rd Sem/PHY-H-CC-T-07/20

U.G. 3rd Semester Examination - 2020

PHYSICS

[HONOURS]

Course Code: PHY-H-CC-T-07

(Digital Systems and Applications)

Full Marks : 40 Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP-A

1. Answer any **five** questions:

 $2 \times 5 = 10$

- a) What is the time base in a CRO? What is the main component of a CRO?
- b) What are analog and digital circuits? Give examples.
- c) What do you mean by bit and byte?
- d) NAND and NOR gates are called universal gateswhy?
- e) Convert the decimal number 23.8125 into its binary equivalent.

- f) What are encoder and decoder?
- g) What is the difference between a sequential logic system and a combinational logic system?
- h) What do you mean by a 8-bit microprocessor?

GROUP-B

2. Answer any two questions:

 $5 \times 2 = 10$

- a) i) Explain how the frequency of an A.C. signal can be measured by a CRO.
 - ii) Explain briefly how a waveform is displayed on the screen of a CRO. 3+2
- b) i) State and prove De Morgan's theorems.
 - ii) Find the hexadecimal equivalent for the decimal number 581. 4+1
- c) i) Verify the Boolean identities:

a)
$$AB + AC + B\overline{C} = AC + B\overline{C}$$

b)
$$AB + \overline{A}C = (A + C) + (\overline{A} + B)$$

- ii) What is a flip-flop? What is its importance in a digital system? 3+(1+1)
- d) i) What are half adder and full adder? Draw the logic block diagram for adding two decimal numbers 7 and 12

ii) What is a demultiplexer? Give the circuit diagram of a 1 -line to 4-line demultiplexer using basic gates. 3+2

GROUP-C

3. Answer any two questions:

 $10 \times 2 = 20$

- a) i) With the help of a truth table explain the operation of a JK flip-flop having preset and clear input facilities.
 - ii) What is meant by race-around condition? How it can be avoided? What do you mean by edge triggering? 6+(1+1+2)
- b) i) What is a synchronous counter? What is its advantage over asynchronous counter? Draw a block diagram of a 3-bit synchronous counter and explain its operation with the necessary timing diagram.
 - ii) 'An equality detector gives an output if the inputs A and B are both 1 or if A and B are both zero'. Implement the circuit.

(1+1+5)+3

c) i) What do you mean by ROM and RAM? What is a computer bus? What are address bus and

- data bus of a microprocessor? What do you mean by bus width?
- ii) How can a NOT gate be obtained from a NAND gate? Show that an AND gate can be built with NAND gates.

$$(2+1+2+1)+(2+2)$$

- d) i) Subtract (1011)₂ from (11001)₂ and convert the result into the corresponding decimal number. Convert the hexadecimal number C5E2 into a binary number.
 - ii) What is a multivibrator? Name the different classes of multivibrators and briefly distinguish between them. What are **half** and **full** subtractor? (2+2)+(1+3)+2
