# U.G. 2nd Semester Examination - 2021

## COMPUTER SCIENCE

**[HONOURS]**

**Course Code : COM.SC-H-CC-L-204**

**(Computer System Architecture)**

Full Marks : 30 Time : $1\frac{1}{2}$ Hours

*The figures in the right-hand margin indicate marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

### GROUP–A

1. Answer any **five** questions : 2×5=10

   a) Differentiate between computer organization and computer architecture.

   b) State the purpose of using Program Counter.

   c) What do you mean by locality of reference?

   d) What are physical and logical addresses?

   e) Define toggle condition in flip-flop.

   f) Why a multiplexer is called a data selector?

   g) What do you mean by control word?

   h) What is pseudoinstruction?



### GROUP-B

2. Answer any **two** questions : 5×2=10

   a) Show how a J-K flip-flop can be converted to a T flip-flop. Show the steps with proper explanations.

   b) Perform the arithmetic operation in binary using signed 2's complement representation of negative numbers:

   (i) (+42) + (-23) (ii) (-42) + (-23)

   c) Explain the operation of the 4-bit asynchronous counter with diagram.

   d) Convert the BCD to XS-3 and XS-3 to BCD by using a full adder.

   e) What do you understand by the term "Instruction Set Completeness"? How do "memory reference instructions" work?

### GROUP-C

3. Answer any **one** question: 10×1=10

   a) What is an interrupt? Discuss interrupt types and interrupt cycle in brief. 2+4+4

   b) Compare cache writing policies in brief. A computer has an 8 GB memory with 64 bit word sizes. Each block of memory stores 16

words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4-way set associative cache, what is the new address format?

3+3+4

c) Discuss arithmetic pipeline with proper example. Explain the conflicts which happened in instruction pipeline. 4+6

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