U.G. 2nd Semester Examination - 2022

COMPUTER SCIENCE

[PROGRAMME]

Course Code : COM.SC.-G-CC-L-201 B

(Computer System Architecture)

Full Marks : 60 Time : $2\frac{1}{2}$ Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP–A

1. Answer any **ten** questions: 2×10=20

   a) What is immediate addressing mode?

   b) Why is NAND gate called universal gate?

   c) What is the function of program counter?

   d) Define miss penalty.

   e) What do you mean by content addressable memory?

   f) Define locality of reference.

   g) Differentiate between logical address and physical address.

   h) Define microinstruction.

   i) Convert $(1001001.011)_2$ to decimal number.

   j) Subtract the following using 2's complement:

   $$(11010)_2 - (1101)_2$$

   k) Simplify the following Boolean expression:

   $$F = BC + AC' + AB + BCD$$

   l) Obtain the truth table of the function:

   $$F = XY + XY' + Y'Z$$

GROUP–B

2. Answer any **four** questions: 5×4=20

   a) Convert the following expression into one address, two address and three address instruction formats: 2+2+1

   $$F = (A + B) / (C - D)$$

   b) Apply Booth's algorithm to multiply the two numbers $(+3)_{10}$ and $(-3)_{10}$. 5

   c) Explain and draw 4-bit binary *decrementer* circuit. 5

   d) Explain with diagram how you can convert J-K flip flop into T flip flop. 5

e) Write short note on pipeline hazards. 5

f) State De-Morgan's laws in Boolean algebra. Also prove De-Morgan's laws using Truth table. 2+3

g) Differentiate between RISC and CISC architecture in detail. 5

GROUP–C

3. Answer any **two** questions: 10×2=20

a) Define cache memory. Why a DRAM cell needs refreshing? Given the following, determine size of the sub-fields (in bits) in the address for the direct mapping, associative and set associative mapping cache schemes: We have 256 MB main memory and 1 MB cache memory. The address space of this processor is 256 MB. The block size is 128 bytes. There are 8 blocks in a cache set. 2+2+6

b) Represent the decimal value (–3.75) in IEEE 754 single precision floating-point format. Define guard bit. Explain the operation of 4-bit asynchronous counter. 3+2+5

c) Discuss about the basic functional components of CPU in brief. State the purpose of memory address register (MAR) and stack pointer (SP). 6+2+2

d) Write short notes (any **two**): 5+5

i) Memory hierarchy

ii) DMA

iii) Multiplexer

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